IN THE CLAIMS

1. (Currently amended) A method of classifying defect chips, said method comprising:

finding defect locations on a wafer using a semiconductor defect inspection instrument;

analyzing the defect composition using the semiconductor defect inspection instrument; and

marking defect locations on a wafer map using ~~the~~ different types of marks to identify of different types of defects.

2. (Currently amended) The method according to claim 1, wherein the different types of marks differ according to shape.

3. (Currently amended) The method according to claim 1, wherein the different types of marks are color differ according to color.

4. (Original) The method according to claim 1, further comprising graphing defect characteristics concurrently with marking defect locations on the wafer map.

5. (Original) The method according to claim 1, further comprising storing and analyzing defect characteristics electronically using software.

6. (Original) The method according to claim 1, further comprising:
using the marks on the wafer map to prepare graphs to assist in statistically analyzing the defects.

7. (Original) A wafer defect map, comprising:

a schematic representation of a semiconductor wafer, including demarcations corresponding to the location of chip boundaries; and

a plurality of markings, each marking corresponding to a wafer defect,

wherein locations of the markings on the wafer map correspond to locations of the defects on the wafer, and wherein each marking is configured to identify a type of defect.

8. (Previously presented) The wafer defect map according to claim 7, wherein each marking is configured to identify a type of defect by using a color that is associated with that type of defect.

9. (Original) The wafer defect map according to claim 7, wherein the markings have different shapes depending on defect type.

10. (Original) The wafer defect map according to claim 7, wherein the location and type of wafer defects is determined using a semiconductor defect inspection instrument.

11. (Original) A method of statistically analyzing defects on a semiconductor wafer to improve yield, said method comprising:

identifying a location and type of wafer defects;

determining a composition of the wafer defects;

preparing a wafer defect map to visually represent the location and type of the wafer defects; and

preparing one or more charts and/or graphs to statistically represent defect characteristics.

12. (Original) The method according to claim 11, wherein markings are placed on the wafer defect map corresponding to defect locations.

13. (Previously presented) The method according to claim 12, wherein preparing a wafer defect map to visually represent the location and type of the wafer defects comprises: using marks on the wafer defect map that are assigned a color based upon the type of the wafer defect.

14. (Original) The method according to claim 11, wherein identifying a location and type of wafer defects comprises using an optical or scanning electron microscope to identify the location and type of wafer defects.

15. (Original) The method according to claim 11, wherein determining a composition of the wafer defects comprises performing an AES analysis on the defects to determine the compositions thereof.

16. (Original) The method according to claim 11, wherein preparing one or more charts and/or graphs comprises constructing a table comprising columns corresponding to defect type, defect composition, defect cause, and defect location.

17. (Original) The method according to claim 11, wherein preparing one or more charts and/or graphs comprises preparing a bar graphs representing the number of defects according to defect type.

18. (Original) The method according to claim 11, wherein preparing a wafer defect map to visually represent the location and type of the wafer defects, and preparing one or more charts or graphs to statistically represent defect characteristics are performed electronically.

19. (Original) The method according to claim 18, wherein identifying a location and type of wafer defects, and determining a composition of the wafer defects are also performed electronically.

20. (Original) The method according to claim 11, further comprising analyzing the one or more charts or graphs to determine appropriate corrective action in a wafer fabrication process.